REMARKS

Claims 1-9 and 11-40 are pending in the present application.

The Examiner stated that Claims 36-38 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. Applicant has not amended claims 36-38 because Applicant believes, for the reasons set forth below, that base Claim 27 is allowable.

By way of example with reference to Figs. 10 and 11, an embodiment of the invention teaches a memory subsystem equipped with a first data transfer interface 1106a coupled to an array of memory cells 1102 to provide a first access path for a processor and a subsystem, a second data transfer interface coupled to the array of memory cells to provide a second access path 112 for the processor to access the array of memory cells, and a controller coupled to the array of memory cells and the first and second data transfer interfaces to control access to the array of memory cells. Access is granted to the second data transfer interface prior to granting access to the first data transfer interface.

Claims 1-4, 6-9, 11-20, 22-29, 31-35 and 39 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen (US5197130) in view of Grace (US6560160). The rejection is respectfully traversed.

Chen describes a cluster architecture for a highly parallel multiprocessor computer processing system. The system includes one or more clusters of tightly-coupled, high-speed processors capable of both vector and scalar parallel processing that can symmetrically access shared resources associated with the cluster, as well as the shared resources associated with other clusters. The Examiner acknowledges that Chen does not teach a second data interface having priority over the first data transfer interface. Indeed, Chen describes a "first-come-first-served" priority scheme and although this scheme includes priority data, it in no way suggests priority is given to the second data interface over the first data interface. Rather, Chen would use the highest priority request no matter where the request came from.

The Examiner cites Grace for teaching a second data transfer interface having priority over the first data transfer interface. In support, the Examiner refers to column 4, lines 31-37 of Grace. Referring to the entire paragraph, that section of Grace states:

> At time t10, the control circuit 116 detects the PortA access from signals on the control portion 120 and then at time t20 detects the PortB access from signals on the control portion 130. After time t10, the control circuit 116 issues the control signal 140 to select the address held in the address latch 110 since the PortA access was received first. At time t30, the control circuit 116 asserts the Port_Controls as appropriate to carry out the PortA access. During the PortA access, the PortB access is held waiting for completion of the PortA access. After completion of the PortA access, the control circuit 116 issues the control signal 140 to select the address held in the address latch 112 and then at time t40 asserts the Port_Controls as appropriate to carry out the PortB access. (col. 4, lines 24-37, emphasis added)

The inference that the Examiner appears to be taking from this section of Grace is that PortA is being given priority over PortB. However, as stated at line 29, this is simply due to the fact that the PortA access was received first. Indeed, Grace further states:

> This is only one example and numerous other combinations of sequences are possible. For example, the PortA and PortB accesses may occur at the same time or the PortB access may precede the PortA access in which case the control circuit 116 carries out the PortB access and then the PortA access. The PortA access may be a read and the PortB access a write or visa versa. If the PortA and PortB accesses occur at the same time then the control circuit 116 selects one or the other to be sequenced first to the array 24. (col. 4, lines 59-67, emphasis added)

The foregoing indicates that Grace grants access between PortA and PortB simply based on timing of accesses by the respective ports. Thus, Grace teaches nothing about "the second data transfer interface having priority over the first data transfer interface" as required by base claim 1. Chen and Grace, alone or in combination, do not teach, suggest, or otherwise make obvious this limitation. Applicants respectfully request withdrawal of the rejection of base claim 1 under section 103(a).

Dependent claims 2-4, 6, 7, and 39 depend from allowable base claim 1 and are allowable for the same reasons. Applicants respectfully request withdrawal of the rejection of dependent Claims 2-4, 6, 7, and 39 under section 103(a).

Base claims 8, 16, and 27 include similar limitations as recited in base claim 1 and are allowable for the same reasons. Claims 9, 11-15, 17-20, 22-26 and 28-29 which depend from base claims 8, 16 and 27, respectively are allowable for the same reasons. Applicants

respectfully request withdrawal of the rejection of claims 8-9, 11-20, and 22-29 under section 103(a).

Claims 5, 21, and 30 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Agarwala (US6681270). The rejection is respectfully traversed.

Agarwala describes a data transfer controller that uses an effective channel priority processing technique and algorithm. Data transfer requests are queued in a first-in-first-out fashion at the data source ports. This technique prevents a low priority data transfer request at the output of a source port queue from blocking a higher priority data transfer request further back in the same port. Agarwala does not teach a second data interface having priority over the first data transfer interface. In contrast, like Chen, Agarwala utilizes a "first-in-first-out" priority scheme and although this scheme includes priority data, it in no way suggests priority is given to the second data interface over the first data interface. Rather, Agarwala would use the highest priority request no matter where the request came from.

Neither Chen or Agarwala, alone or in combination, teaches, suggests, or otherwise makes obvious the limitations as recited in claim 5. Claim 5 depends from allowable claim 1 and is allowable for the same reasons. Applicant respectfully requests the withdrawal of the rejection of claim 5 under section 103.

As noted above, base claims 16 and 27 include similar limitations as claim 1 and are allowable for the same reasons. Claims 21 and 30 depend from claims 16 and 27, respectively, and are allowable for the same reasons. Applicant respectfully requests the withdrawal of the rejection of claims 21 and 30 under section 103.

Claims 40 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen and Grace, in view of Mulla (US6557078). The rejection is respectfully traversed.

Mulla describes a cache using a queuing structure that provides out-of-order cache memory access support for multiple accesses, as well as support for managing bank conflicts and address conflicts. Mulla does not teach a second data interface having priority over the first data transfer interface.

As stated above, the limitation in claim 1 that recites "the second data transfer interface having priority over the first data transfer interface" is not taught or suggested by the combination of Chen and Grace. Chen and Mulla, alone or in combination, do not teach,

suggest, or otherwise make obvious this limitation. Claim 40 depends from claim 1 and is allowable for the same reasons. Applicant respectfully requests the withdrawal of the rejection of claim 40 under section 103.

CONCLUSION

In view of the above remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

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